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LSI Docket No. 02-6050

Remarks/Arguments

In the Final Office Action mailed on 7 November 2006, the Examiner rejected claims 1-6 and 8-22 under 35 U.S.C. §102(b) as anticipated by Shinozaki (United States Patent Number 6,333,875).

Applicants respectfully traverse the rejection and request reconsideration and withdrawal of same. Claims 1, 8, 13 and 18 have been amended for editorial clarity and to better protect the invention. Applicants have added new claims 24 and 25, which recite that the first and second circuitry comprise substantially the same circuitry. Antecedent basis for this limitation may be found on page 9, lines 19-21 of the specification.

35 U.S.C. §102(b) Rejection

The Examiner rejected claims 1-6 and 8-22 under 35 U.S.C. §102(b) as anticipated by Shinozaki. The rejection will be discussed in regard to independent claim 1.

Claim 1 is directed at a system for latching data. Present day circuits have overhead delays caused by fabrication process variations and operating conditions of the circuit. These overhead delays may vary across the surface of the circuit, leading to varying delays at different physical locations of the integrated circuit die. Thus, a delayed signal generated at one physical location of the circuit with a particular designed delay value may be delayed due to local overhead variations in comparison with similarly delayed signals generated elsewhere on the circuit designed with the same delay value. The local overhead variation adds additional delay to the designed delay, causing the actual delay to be higher than the designed delay. As circuit speeds have increased, this overhead delay has become a measurable portion of the intended programmed delays. Thus, the overhead delay may cause timing errors such as when clocking data signals. Therefore, a data signal and a strobe signal may not be properly aligned, and data corruption may occur.

The system of amended claim 1 solves this problem by providing a first delay circuit configured for programmably delaying a strobe signal with a first delay to latch an associated data signal. The first delay circuit has an overhead delay that varies based on

fabrication process variations or operating conditions of the first delay circuit. As a result, the overhead delay effectively adds to the programmed first delay by the amount of time of the overhead delay. A second delay circuit in close proximity to the first delay circuit delays the data signal with a second delay. Because the second delay circuit is in close proximity to the first delay circuit, the second delay circuit has substantially identical fabrication process variations and/or operating conditions as the first delay circuit. These identical process variations and operating conditions generate substantially the same overhead delay in the first and second delay circuits. The second delay is then substantially identical to the overhead delay of the first circuit. Thus, the second delay circuit is able to effectively compensate for the associated overhead delay from the first delay so that the strobe signal and data signal are properly aligned.

By contrast, Shinozaki discloses a semiconductor circuit which receives a strobe signal and a data signal. The circuit includes a latch-signal-generation circuit which generates a first latch signal delay by a first delay time relative to the strobe signal and a second latch signal inverted and delayed by a second delay time relative to the strobe signal. A control circuit adaptively controls the latch-signal-generation circuit to adjust timings of the first and second latch signals such that the first delay time and the second delay time become substantially equal. The data signal is then latched at edge timings of the first and second latch signals. Thus, the strobe signals are created with delays substantially equal for latching a data signal at rising and falling edges of a clock signal (see Abstract of Shinozaki).

Shinozaki does not disclose nor reasonably suggest two delay circuits in close proximity for generating delays of a strobe signal and a data signal with substantially identical overhead delays, where the close proximity of the two delay circuits generates the same overhead delay in both delay circuits. The close proximity of the first and second delay circuits in claim 1 of the present application allows the second delay circuit to effectively compensate for the overhead delay of the first delay circuit using the inherent overhead delay in the second circuit.

The Examiner states that the close proximity recitation is taught by FIG. 3 of Shinozaki. While FIG. 3 of Shinozaki shows delay circuit 28 and latch-signal-generation-circuit 35 in physical proximity in relation to other elements of the figure,

Shinozaki does not teach or reasonably suggest that delay circuit 28 and latch-signal-generation-circuit 35 have identical or even similar overhead delays due to their proximity to each other. In other words, the proximity of elements of the figure is not a teaching that there is any requirement for, or benefit from fabricating the two circuits in close proximity. Rather, Shinozaki teaches that a control circuit (e.g., latch-signal-generation-control circuit 35) is needed to adaptively control and adjust timings of first and second latch signals such that the first delay time and the second delay time become substantially equal (Shinozaki col. 2, lines 58-64). Shinozaki discloses creating adjustable delays *ta* and *tb* such that the difference between the two delays is substantially zero (e.g., within a specific tolerance) (Shinozaki, col. 4, lines 8-21). If the difference between delays *ta* and *tb* is not zero, then a programmable delay is used to adjust the difference. Thus, Shinozaki uses a feedback loop and several programmable delays to equalize the difference between the delays, allowing multiple latch signals to be aligned with rising and falling edges of the strobe signal. If delay circuit 28 and latch-signal-generation-control circuit 35 of Shinozaki had the same overhead delay, then the adjustable timing would not be needed to synchronize the two delays. Thus, Shinozaki offers no suggestion or motivation (let alone any teaching) of a need for, or benefit from fabrication of the two delay circuits in close proximity.

Amended claim 1 of the present application also recites that the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations and operating conditions of the first delay circuit. This overhead delay may be localized, and may cause data signals and strobe signals to be mis-aligned and out of synchronization. A second delay is used with a similar overhead delay to delay the data signal and align the data signal with the strobe signal. Shinozaki does not disclose delaying the data signal with a second delay circuit having an overhead delay that is substantially similar to the overhead delay of the first delay circuit. While Shinozaki does show a delay circuit on the data signal pathway, the delay circuit is not shown to have an overhead delay identical to an overhead delay of another delay circuit associated with the strobe signal. Further, the delay generated by the delay circuit in the data signal pathway of Shinozaki does not appear to be dependent on delays in other functional elements of the circuit (e.g., the latch signal pathway).

By contrast, Shinozaki discloses creating a dummy-variable circuit for emulating delays of rising edges of the input data signal (col. 13, lines 1-5). The comparison circuit 160 of Shinozaki then can adjust a delay of the variable-delay circuit 155 on the data input signal pathway. However, the adjustable delay is based on emulation of an identically configured signal pathway and not on compensation for overhead delays of other signal pathways carrying different signals in close physical proximity. Thus, Shinozaki discloses a different approach and structure for creating delays on the data signal pathway.

Shinozaki discloses that the dummy circuit has the same configuration as the input circuit (col. 6, lines 30-32), and that another dummy circuit has the same configuration as the delay circuit (col. 6, lines 37-39). However, these circuits are not equivalent to the first and second delay circuits of the presently claimed system. Specifically, the dummy circuits do not apply a delay to active signals of the circuit. Rather the dummy circuits emulate delays to allow the comparison circuit to adjust the delays of the delay circuit and the input circuit. Additionally, Shinozaki does not disclose circuits comprising overhead delays, nor does Shinozaki disclose differing delay circuits having equal overhead delays.

In view of the above discussion, Applicants maintain that amended independent claim 1 is distinguished over the teachings of Shinozaki. The claims are neither taught nor reasonably suggested by the teachings of Shinozaki considered alone or by any art of record, considered individually or in any combination. Applicants maintain that independent claims 8, 13 and 18 are distinguished for at least the same reasons discussed above.

Dependent claims 2-6, 9-12, 14-17, 19-22 and 24-25 are allowable for at least the same reasons and as dependent upon allowable base claims. Additionally, dependent claims 2-6, 9-12, 14-17, 19-22 and 24-25 recite additional limitations not found in the prior art of record. Applicants respectfully request reconsideration and withdrawal of the outstanding rejection of claims 1-6 and 8-22. Applicants also respectfully request allowance of new claims 24-25, which recite that the first and second delay circuitry comprise substantially the same circuitry. These features are not shown by the prior art of record.

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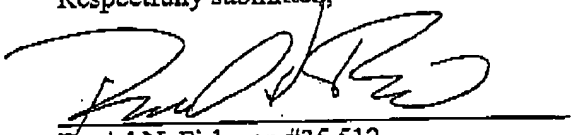
Conclusion

Applicants have amended independent claims 1, 8, 13 and 18 for editorial clarity and to better protect the invention. Applicants have added new claims 24-25. The Examiner's rejection of all claims 1-6 and 8-22 has been thoroughly discussed. Applicants have requested reconsideration and withdrawal of the outstanding rejection and allowance of claims 1-6, 8-22 and 24-25.

Applicants believe that no other fees are due in this matter. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,



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